



New Product

Si4946BEY

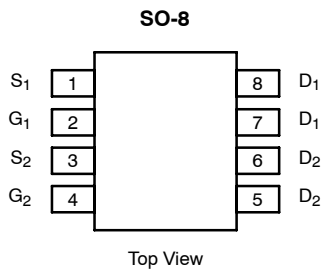
Vishay Siliconix

Dual N-Channel 60-V (D-S) 175 °C MOSFET

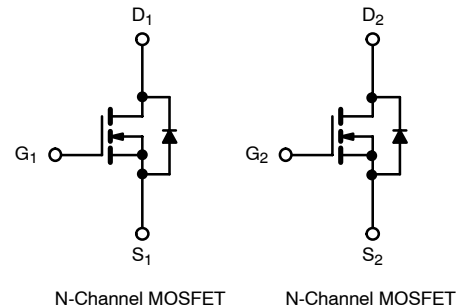
PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
60	0.041 @ V _{GS} = 10 V	6.5	9.2 nC
	0.052 @ V _{GS} = 4.5 V	5.8	

FEATURES

- TrenchFET® Power MOSFET
- 175 °C Maximum Junction Temperature
- 100% R_g Tested



Ordering Information: Si4946BEY-T1—E3 (Lead (Pb)-Free)



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current	I _{DM}	30	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	
Avalanche Current	I _{AS}	12	
Single-Pulse Avalanche Energy	E _{AS}	7.2	
Maximum Power Dissipation	P _D	T _C = 25 °C	W
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-50 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R _{thJA}	50	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	33	41	

Notes:

- Surface Mounted on 1" x 1" FR4 Board.
- t = 10 sec
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 110 °C/W.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		53		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			-6.7		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0	2.4	3.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5.3 A		0.033	0.041	Ω
		V _{GS} = 4.5 V, I _D = 4.7 A		0.041	0.052	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5.3 A		24		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		840		pF
Output Capacitance	C _{oss}			71		
Reverse Transfer Capacitance	C _{rss}			44		
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 5.3 A		17	25	nC
		V _{DS} = 30 V, V _{GS} = 5 V, I _D = 5.3 A		9.2	12	
Gate-Source Charge	Q _{gs}			3.3		
Gate-Drain Charge	Q _{gd}		3.7			
Gate Resistance	R _g	f = 1 MHz	3.1	6.5	9.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 6.8 Ω I _D ≅ 4.4 A, V _{GEN} = 4.5 V, R _g = 1 Ω		20	30	ns
Rise Time	t _r			120	180	
Turn-Off Delay Time	t _{d(off)}			20	30	
Fall Time	t _f			30	45	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 6.8 Ω I _D ≅ 4.4 A, V _{GEN} = 10 V, R _g = 1 Ω		10	15	
Rise Time	t _r			12	20	
Turn-Off Delay Time	t _{d(off)}			25	40	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			3.1	A
Pulse Diode Forward Current ^a	I _{SM}				30	
Body Diode Voltage	V _{SD}	I _S = 2 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 4.4 A, di/dt = 100 A/μs, T _J = 25 °C		25	50	ns
Body Diode Reverse Recovery Charge	Q _{rr}			25	50	nC
Reverse Recovery Fall Time	t _a			18		ns
Reverse Recovery Rise Time	t _b			7		

Notes

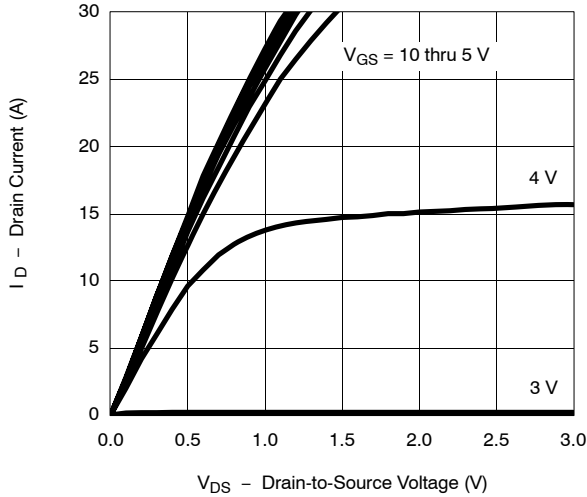
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

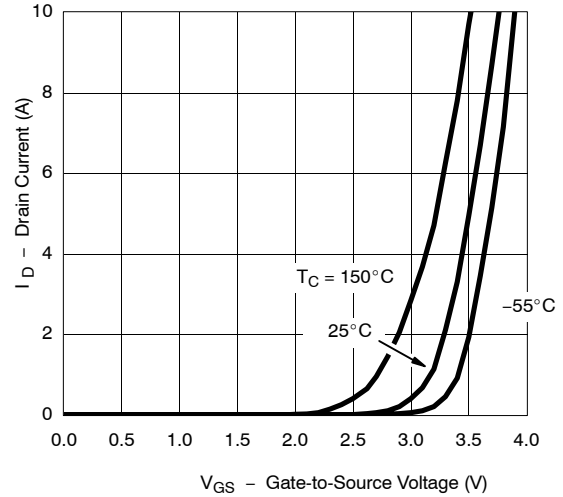


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

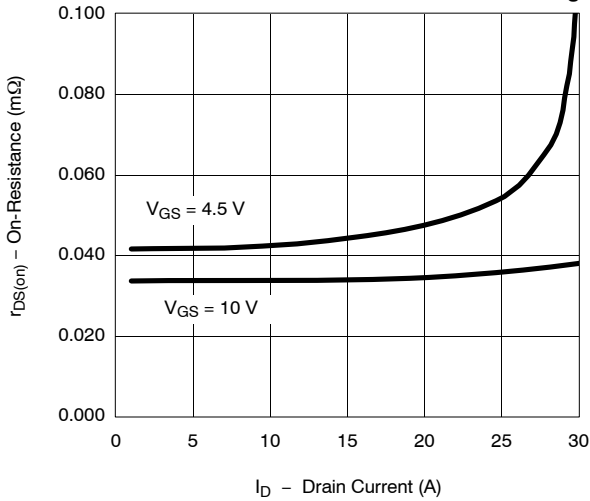
Output Characteristics



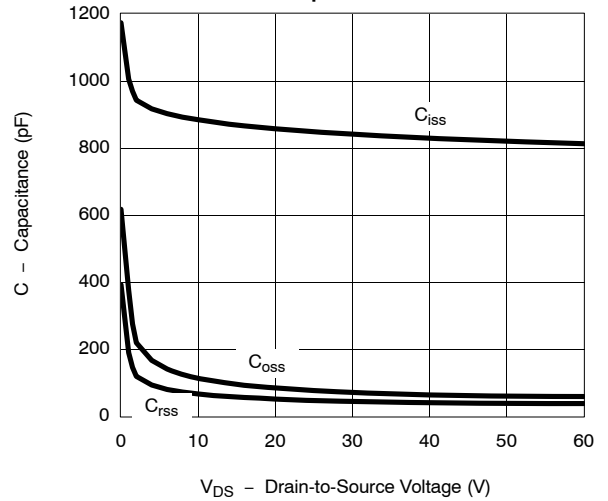
Transfer Characteristics



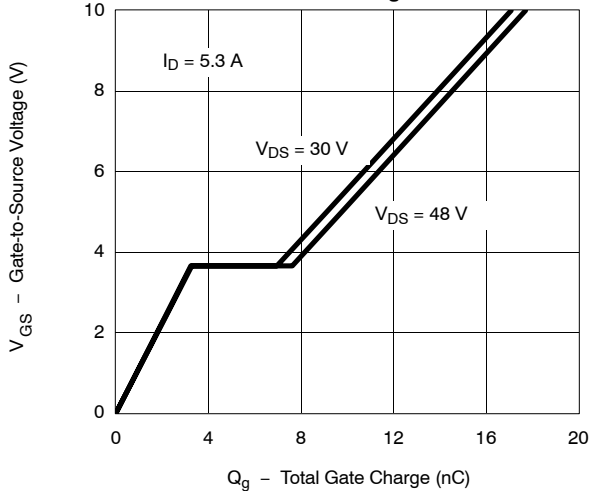
On-Resistance vs. Drain Current and Gate Voltage



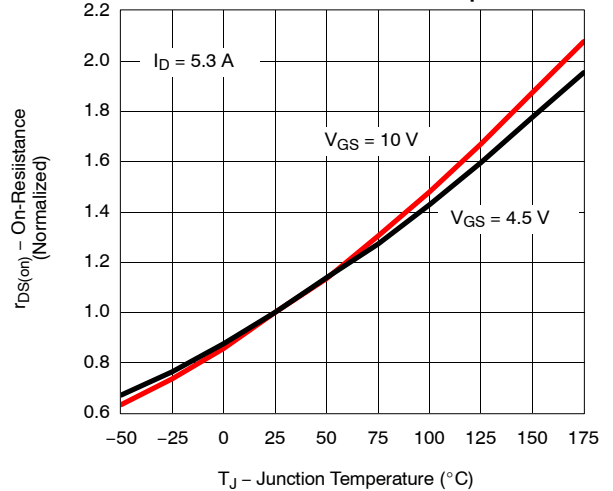
Capacitance



Gate Charge



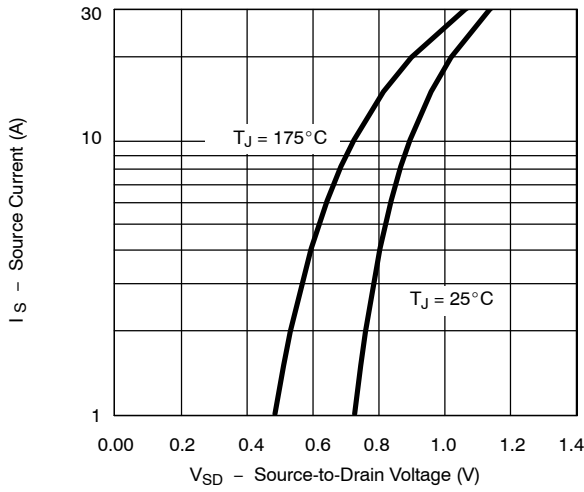
On-Resistance vs. Junction Temperature



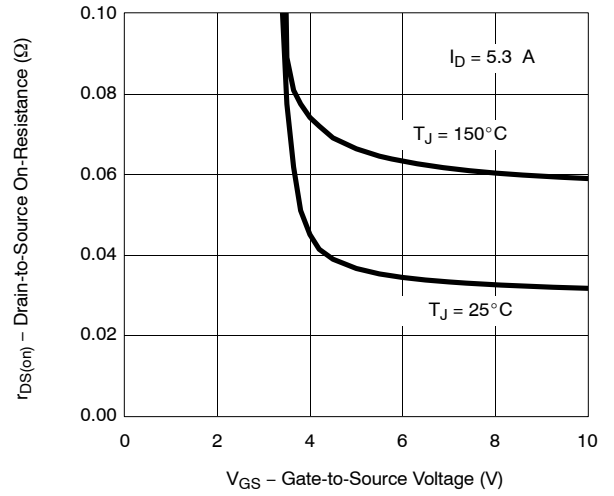


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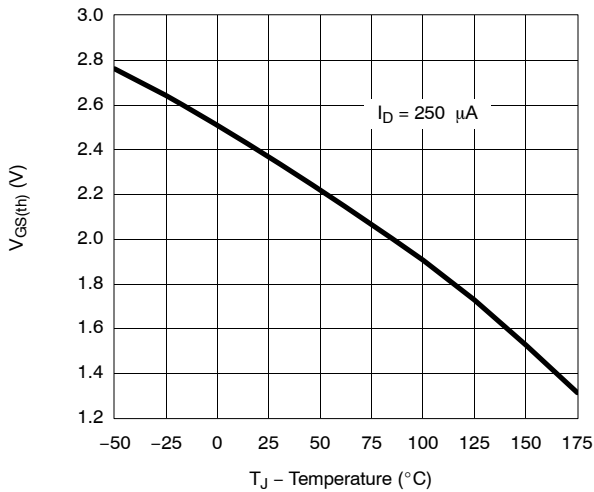
Source-Drain Diode Forward Voltage



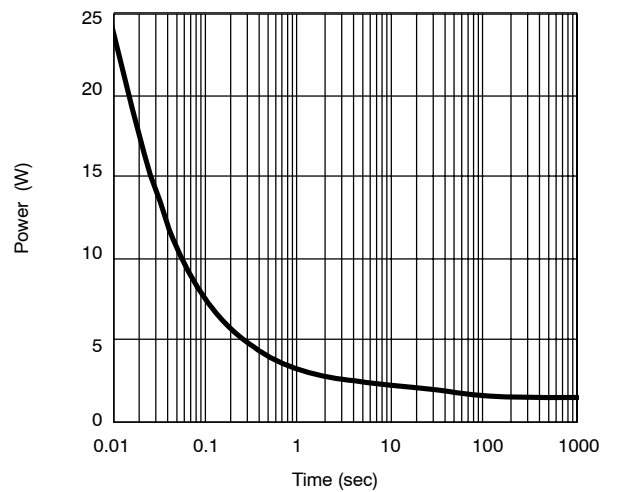
On-Resistance vs. Gate-to-Source Voltage



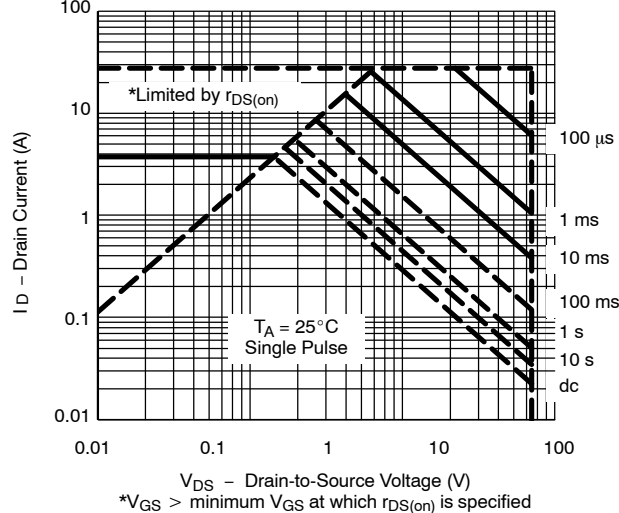
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

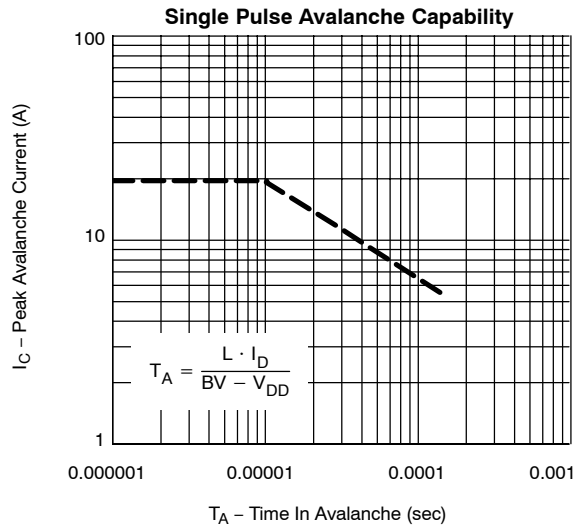
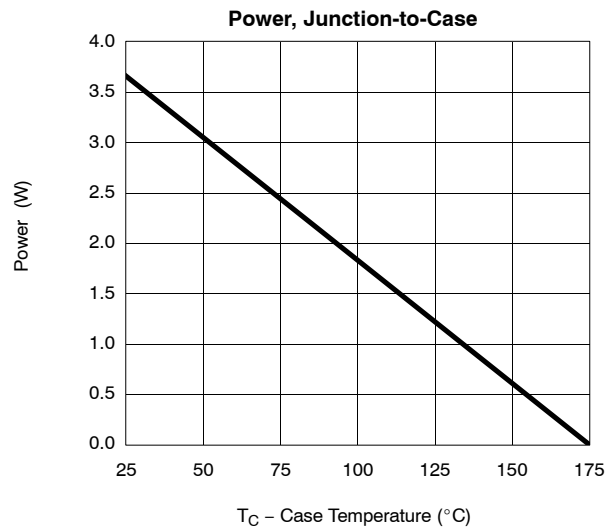
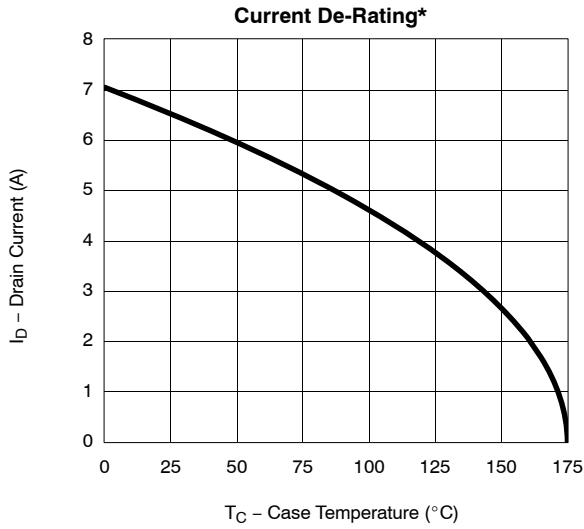


Safe Operating Area, Junction-to-Ambient





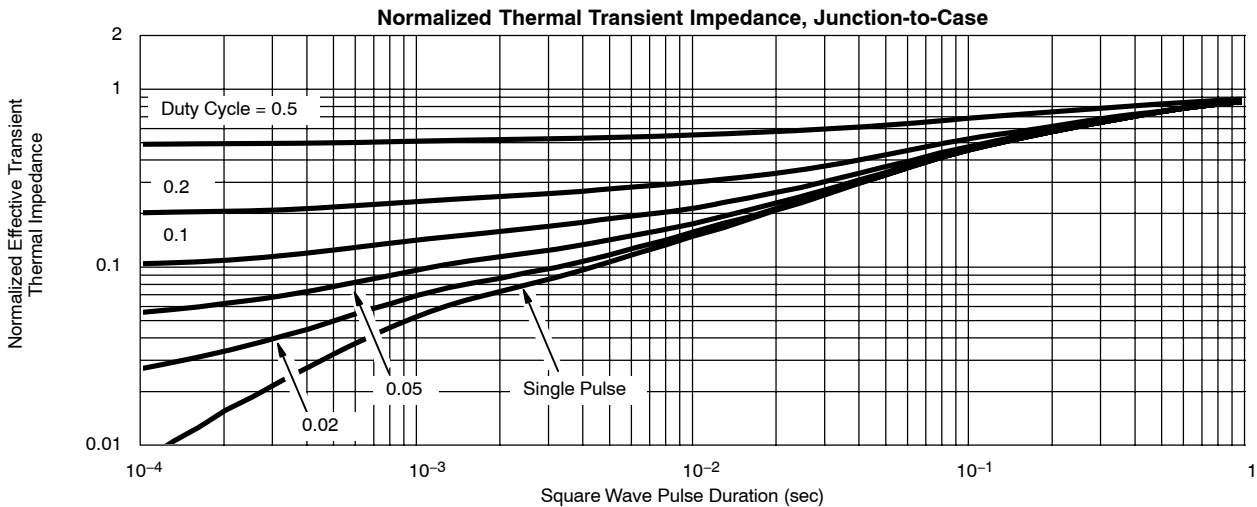
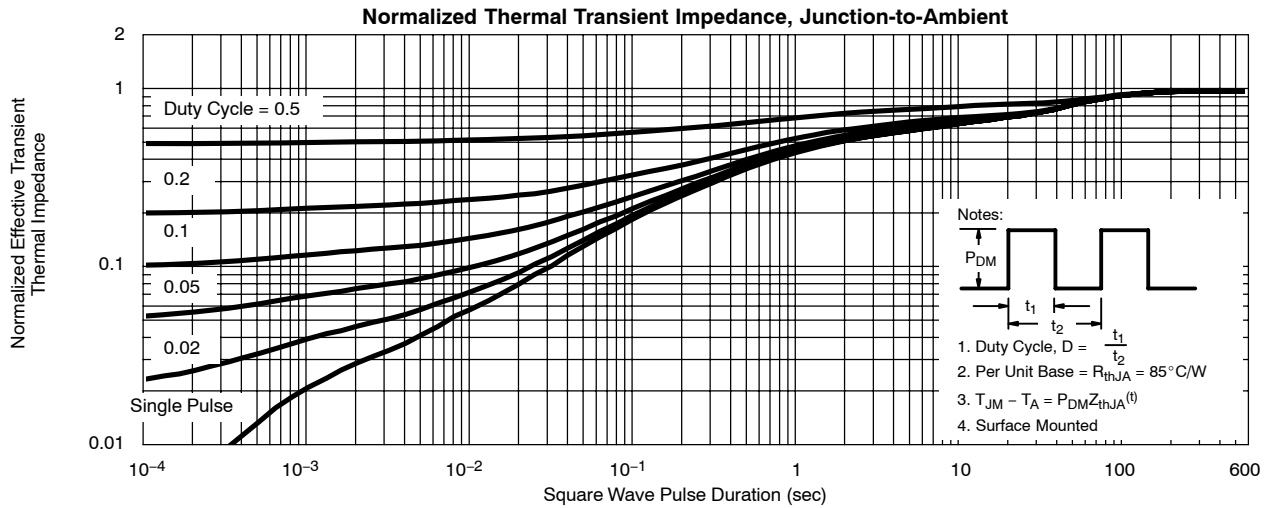
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



*The power dissipation P_D is based on $T_{J(max)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73411>.



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